XILINX®

XC9572 In-System Programmable CPLD

June 1, 1996 (Version 1.0)

Advance Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced 0.6 µm CMOS 5V FastFLASH technology
- Available in 84-pin PLCC, 100-pin PQFP and 100-pin TQFP packages

Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of four 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 1 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

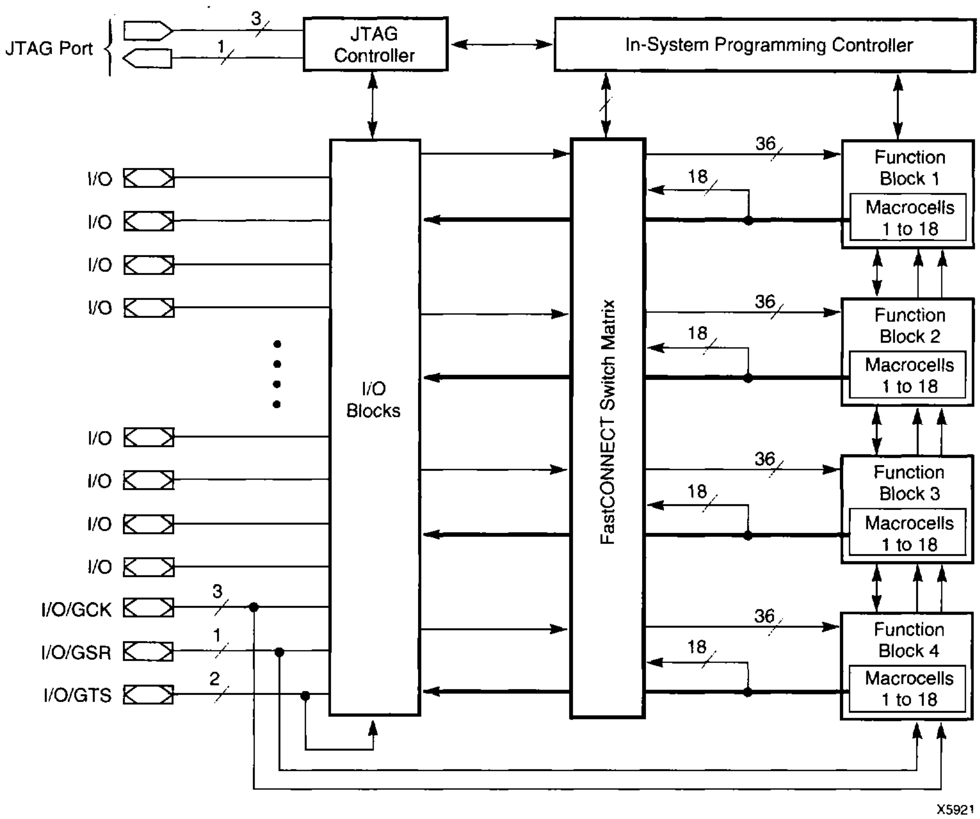

Figure 1: XC9572 Architecture

Note: Function Block outputs indicated by bold line drive directly to I/O Blocks

XC9572 I/O Pins

Function Block	Macrocell	PC84	PQ100	TQ100	BScan Order	Notes	Function Block	Macrocell	PC84	PQ100	TQ100	BScan Order	Notes
1	1	4	18	16	213		3	1	25	43	41	105	
1	2	1	15	13	210		3	2	17	34	32	102	
1	3	6	20	18	207		3	3	31	51	49	99	
1	4	7	22	20	204		3	4	32	52	50	96	
1	5	2	16	14	201		3	5	19	37	35	93	
1	6	3	17	15	198		3	6	34	55	53	90	
1	7	11	27	25	195		3	7	35	56	54	87	
1	8	5	19	17	192		3	8	21	39	37	84	
1	9	9	24	22	189	[1]	3	9	26	44	42	81	
1	10	13	30	28	186		3	10	40	62	60	78	
1	11	10	25	23	183	[1]	3	11	33	54	52	75	
1	12	18	35	33	180		3	12	41	63	61	72	
1	13	20	38	36	177		3	13	43	65	63	69	
1	14	12	29	27	174	[1]	3	14	36	57	55	66	
1	15	14	31	29	171		3	15	37	58	56	63	
1	16	23	41	39	168		3	16	45	67	65	60	
1	17	15	32	30	165		3	17	39	60	58	57	
1	18	24	42	40	162		3	18	–	61	59	54	
2	1	63	89	87	159		4	1	46	68	66	51	
2	2	69	96	94	156		4	2	44	66	64	48	
2	3	67	93	91	153		4	3	51	73	71	45	
2	4	68	95	93	150		4	4	52	74	72	42	
2	5	70	97	95	147		4	5	47	69	67	39	
2	6	71	98	96	144		4	6	54	78	76	36	
2	7	76	5	3	141	[1]	4	7	55	79	77	33	
2	8	72	99	97	138		4	8	48	70	68	30	
2	9	74	1	99	135	[1]	4	9	50	72	70	27	
2	10	75	3	1	132		4	10	57	83	81	24	
2	11	77	6	4	129	[1]	4	11	53	76	74	21	
2	12	79	8	6	126		4	12	58	84	82	18	
2	13	80	10	8	123		4	13	61	87	85	15	
2	14	81	11	9	120		4	14	56	80	78	12	
2	15	83	13	11	117		4	15	65	91	89	9	
2	16	82	12	10	114		4	16	62	88	86	6	
2	17	84	14	12	111		4	17	66	92	90	3	
2	18	–	94	92	108		4	18	–	81	79	0	

Notes: [1] Global control pin

XC9572 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	TQ100
I/O/GCK1	9	24	22
I/O/GCK2	10	25	23
I/O/GCK3	12	29	27
I/O/GTS1	76	5	3
I/O/GTS2	77	6	4
I/O/GSR	74	1	99
TCK	30	50	48
TDI	28	47	45
TDO	59	85	83
TMS	29	49	47
V_{CCINT} 5 V	38,73,78	7,59,100	5,57,98
V_{CCIO} 3.3 V/5 V	22,64	28,40,53,90	26,38,51,88
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	100,21,31,44,62,69,75,84
No Connects	—	4,9,21,26,36,45,48,75,82	2,7,19,24,34,43,46,73,80